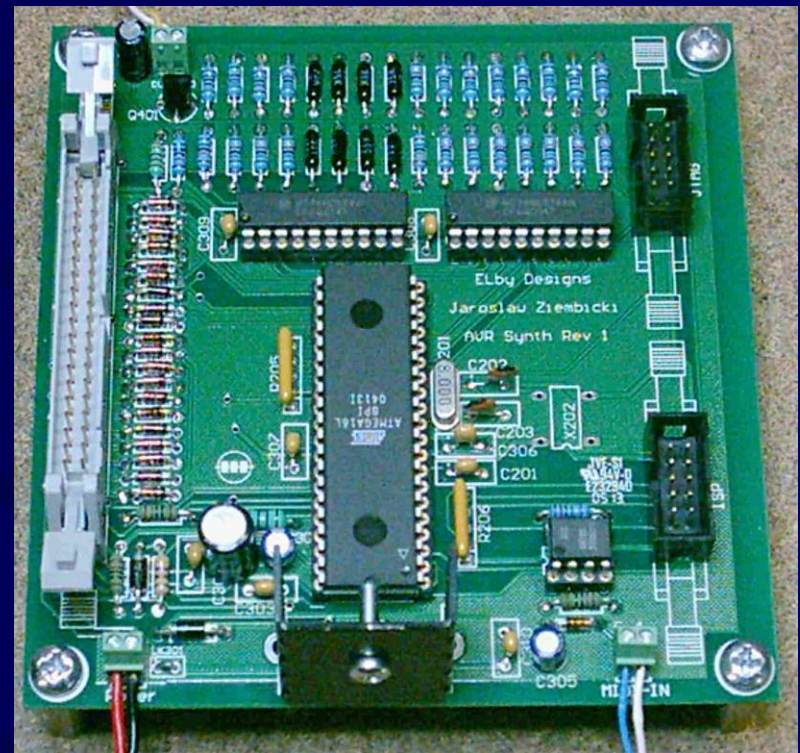# PCB Design & Layout Tips

Ref: Johnson, H., *High-Speed Digital Design.* Prentice Hall, 1993

What is all the extra stuff?

- Power Supply
- Decoupling caps
- Termination resistors
- Mounting holes tied to chassis ground
- All designed to reduce parasitic effects

Ground Distribution

- Solid ground plane is best, provides continuous, low-impedance path for return current

- Absolutely necessary for designs with large amounts of high speed devices (edge rates < 5ns)

- May not be feasible due to budget constraints (Usually requires at least a 4 layer board)
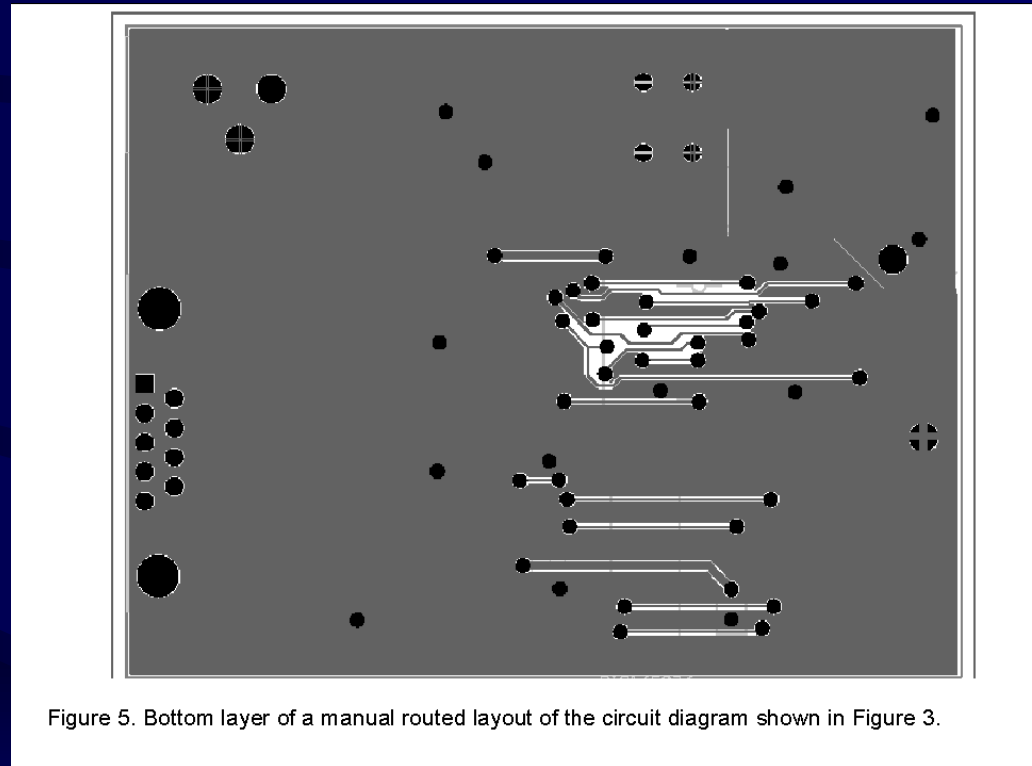
Example solid ground plane layer

- Return current can follow any path and stay close to the signal trace.
- Only breaks in plane are vias and thru holes
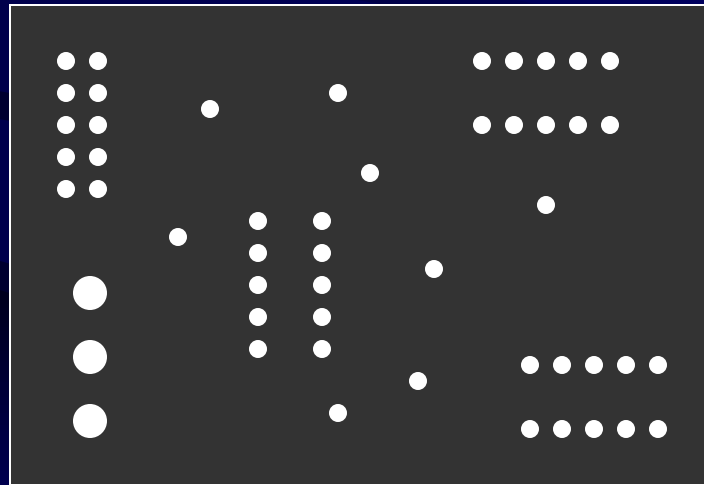
Ground distribution for 2 layer boards

- Try to dedicate one layer as mostly solid ground plane, with routing slots cut out for signal traces
- No traces on the other layer should perpendicularly cross a break in the ground plane (large inductive loop)

Figure 5. Bottom layer of a manual routed layout of the circuit diagram shown in Figure 3.

www.analogzone.com : ACQ_TechNote_052402.pdf

Ground distribution for 2 layer boards – right way

- If most of one layer cannot be dedicated to a ground plane, use a star configuration
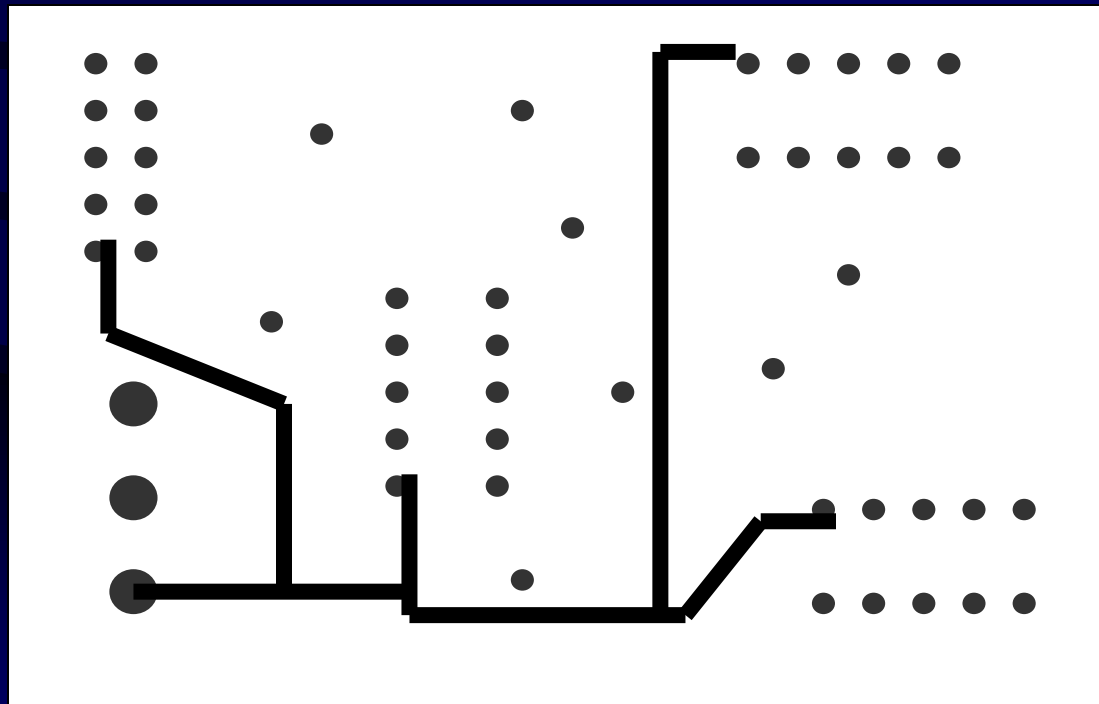
Ground distribution for 2 layer boards – wrong way

- Don't daisy chain all your ground connections together. It forces all return currents to follow the same path, possibly causing ground bounce.
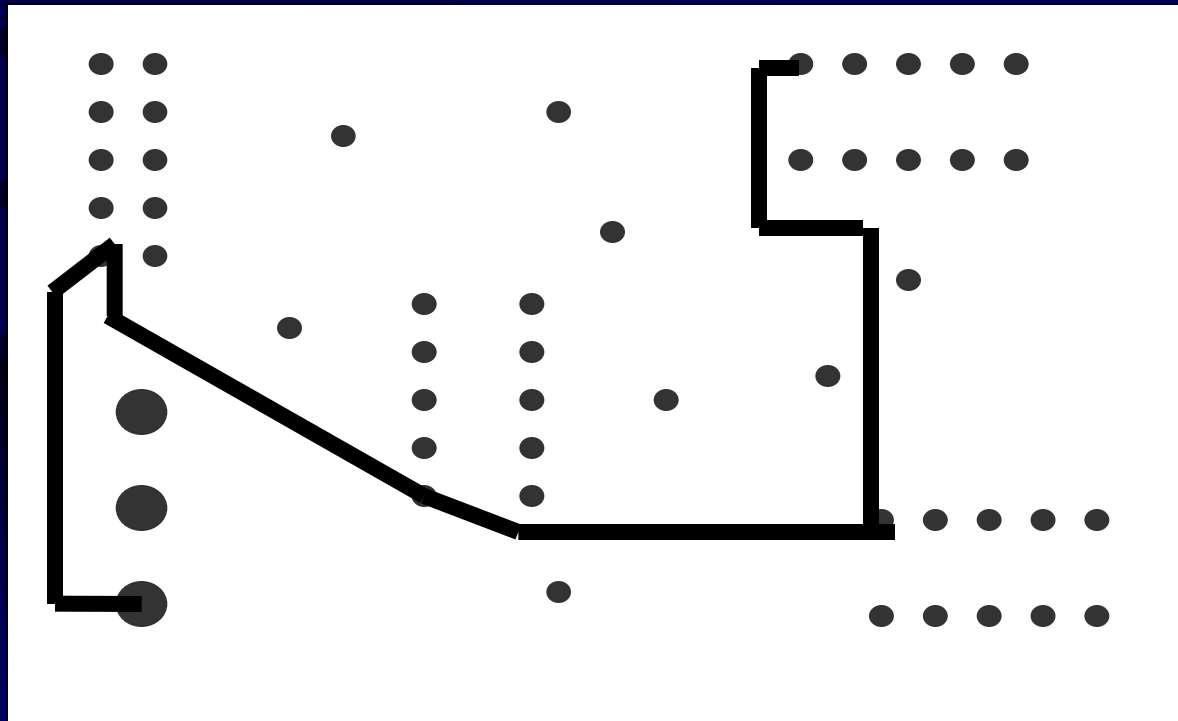
# Ground distribution for 2 layer boards, with mini ground plane

- If a section of the board has ICs with lots of connections and board space allows, draw in a mini ground plane under that section.
- Signals running between these ICs now have a low inductance return path
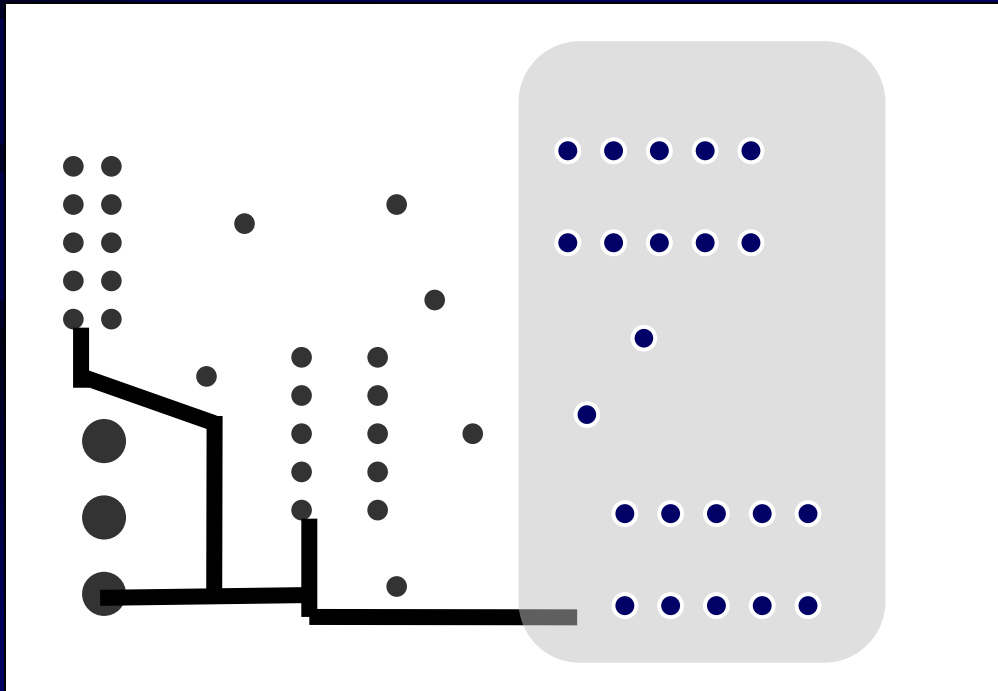
Example solid ground plane w/analog ground

Analog sensor

• Moat in gnd plane, at least 25 mils wide (to prevent capacitive coupling)

• Prevents voltage spikes caused by digital logic from degrading the analog noise margin

• No traces should cross the moat, especially high speed digital ones
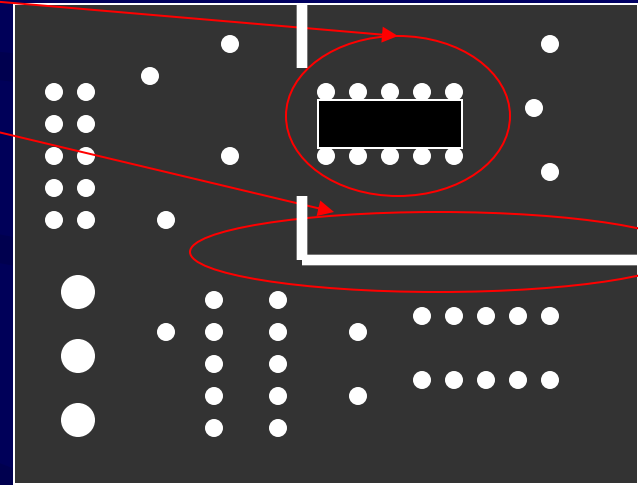
* Tie <u>all</u> gnd pins in the analog region to analog gnd

Mixed voltage designs

- Your design could have as many as 5 or 6 different supply voltages, which will complicate the power distribution routing.
- There are two choices in where to generate the secondary voltages
  - Generate all voltages centrally at the power supply and distribute across the PCB (best when different sections of the board need that voltage)
  - Locate the generation circuit near the components that require that voltage (best if one or two ICs need that voltage)

Mixed voltage designs – interfacing components

- You may have to do some level translation for signals that communicate between two different voltage levels.

- It's important to realize that any level translation <u>wastes</u> power. The customer doesn't care that you had to interface two parts, they only know that the battery has to be recharged too often.

Mixed voltage designs – interfacing components

- To interface a 5V output to a 3.3V input on a slow signal, use a simple voltage divider. Note, however, that these added resistors will slow the rise time of the signal.

- For a faster signal, run the signal through a buffer in the VHC logic family. These parts have 5V tolerant I/O even when powered by 3.3V.

- To interface a 3.3V output to a 5V input, run the signal through a buffer in the HCT product family. These parts have a TTL input stage with a V_{ih} spec of 2V.

Decoupling capacitors

- Main purpose is to act as temporary charge reservoirs, guarding against voltage droop.
- Also serve as a path for high speed return current to jump from Vcc to Gnd (remember, to an AC signal, both Vcc and Gnd are AC gnd).
- Use 10 - 100 uF for bulk decoupling.
- Use 0.01 - 0.1 uF at each power pin (determined by switching frequencies used in design).
- Select a voltage rating higher than Vcc.
- Don't go overboard with too many caps, it will increase cost and decrease available board area.
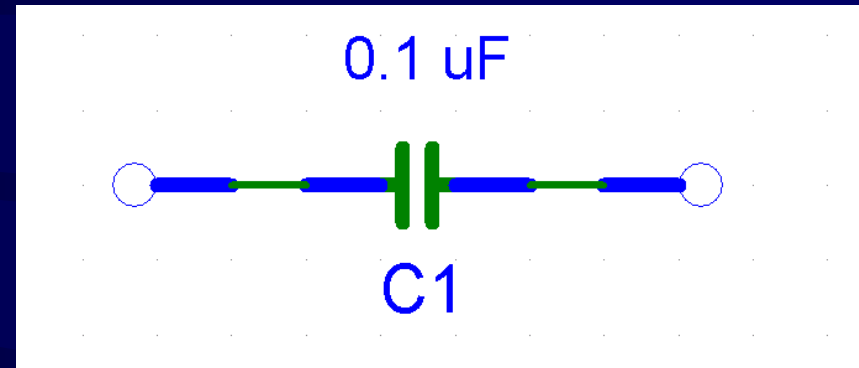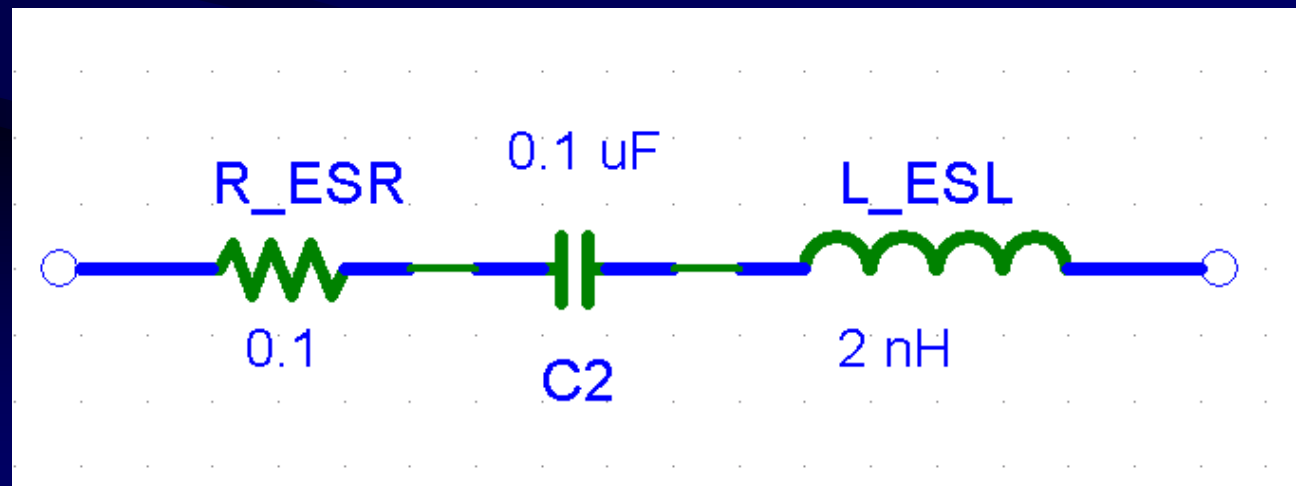
Decoupling capacitor example
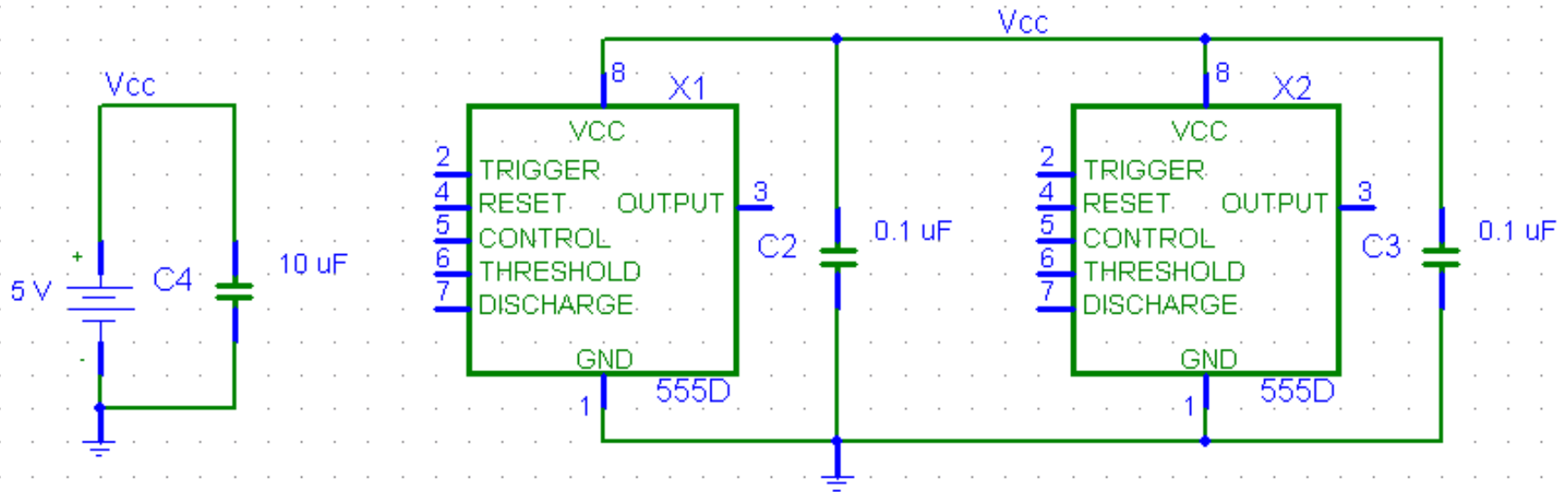
- Here is an example board with two 555 timers (assume that each IC is several inches away from the power supply)
- The 0.1 uF cap supplies current to the IC while its outputs are switching until the power supply can "catch up".
- The large 10 uF capacitor helps recharge all the individual 0.1 uF caps

Decoupling capacitor selection

- You thought the cap you just put in your design looked like this:


- It actually looks like this:

Decoupling capacitor selection

- Two parasitic effects must be considered when selecting decoupling caps. As with most parasitic effects, they are hard to measure, and no two manufacturers seem to report them the same.
    - Equivalent Series Resistance (ESR) : This value will be about the same for thru-hole or SMT packages.
    - Equivalent Series Inductance (ESL) : This value will be much lower for SMT parts, compared to thru-hole.
- These parameters will limit the amount of instantaneous current the cap can supply. Check the cap's datasheet and make sure that neither parameter is unacceptable for your design.

Decoupling capacitor types

- Ceramic
  - Usually have the lowest ESR/ESL
  - Lowest cost
  - Are only recently available in values over 100 uF
- Tantalum
  - Available in a higher capacitance range than ceramic, in the 220 uF – 1000 uF range
  - More expensive, tantalum is rare
  - Polarized, and have a tendency to explode
  - Used to be the first choice for large value decoupling, but ceramics have improved

Filtered power
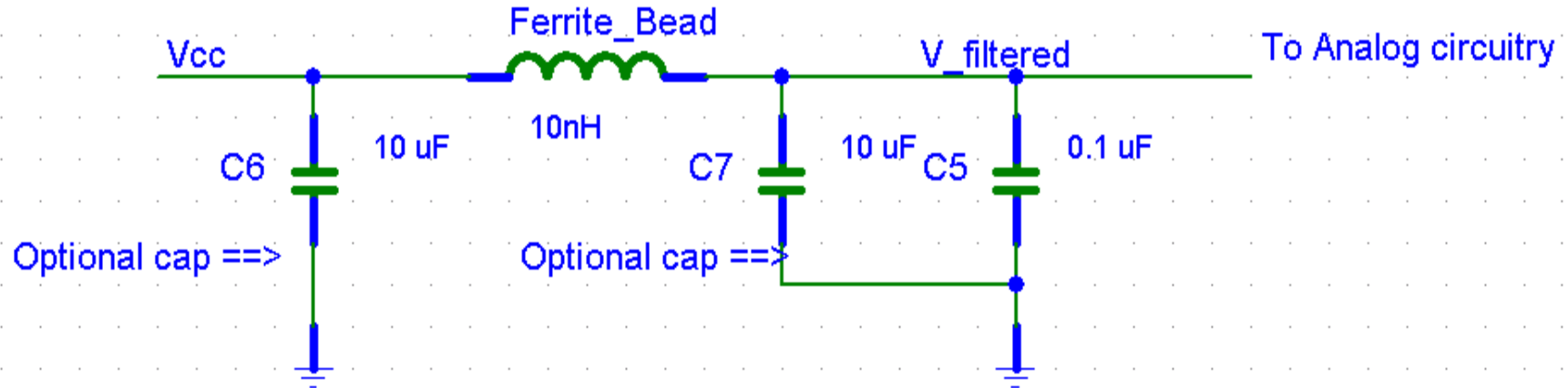
- Some components, especially PLL's or others with analog functions, may require very low ripple on the power rail.

- One solution is to low pass filter the power rail with decoupling caps and ferrite beads (inductors).
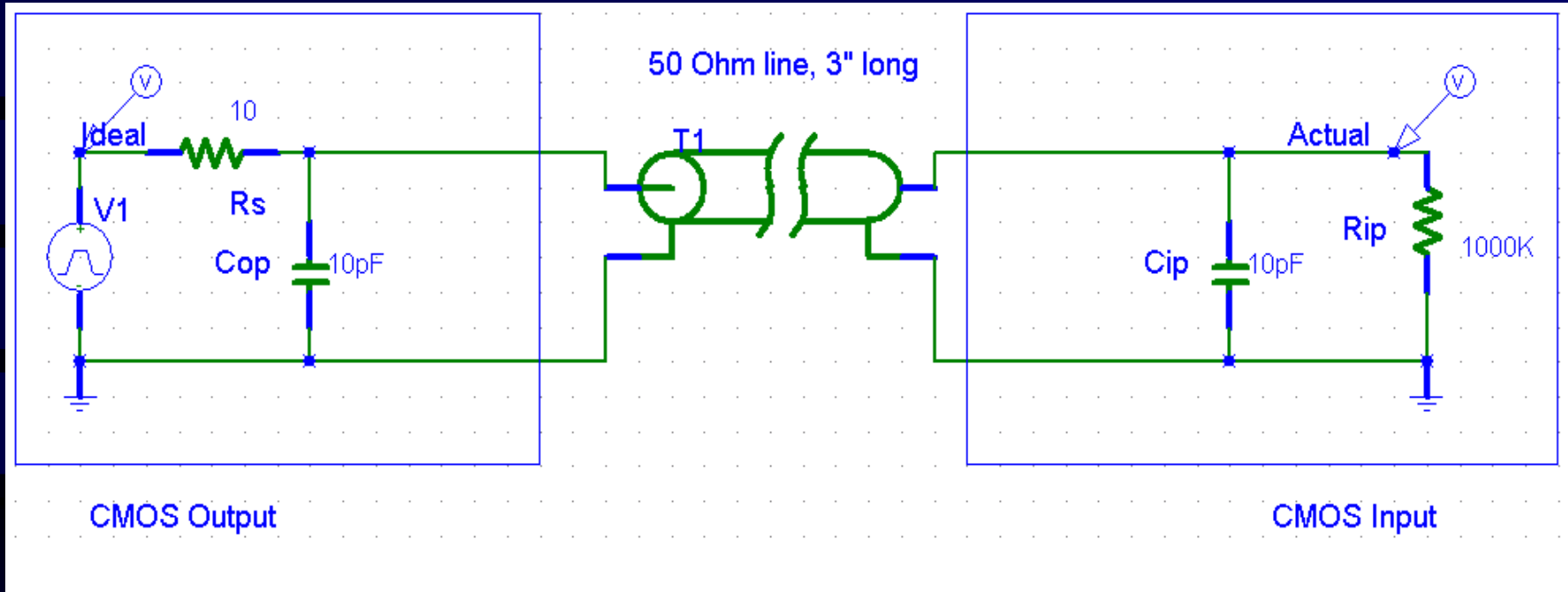
Transmission Line Effects

- The connection from the output of one chip, across the board to the input of another chip is not a superconductor, it's a transmission line with parasitic parameters.

- These effects must be considered for signals with fast rise times and/or long traces.

  10 ns rise time :   12 in

  1 ns rise time   :   1.2 in

Transmission Line Model

Transmission Line Effects

- Here is the resulting simulation, note the overshoot and undershoot (rise time = 5 ns).
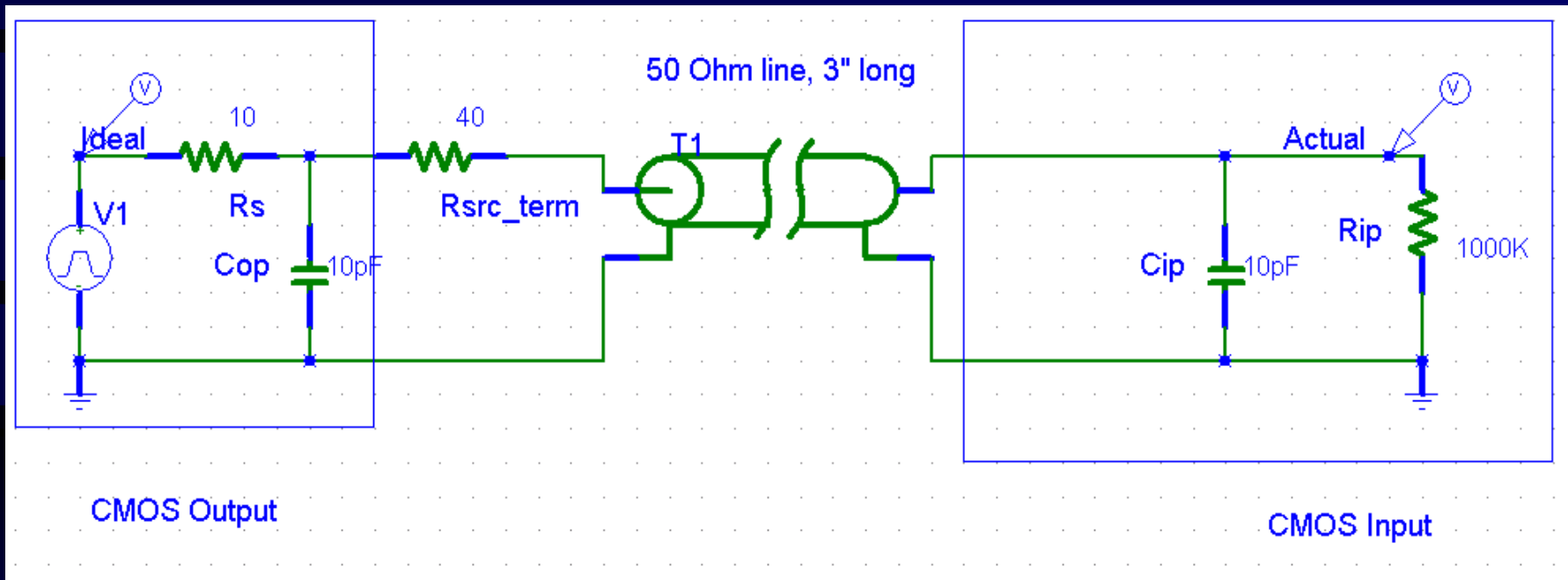
Transmission Line Source Termination

- One resistor in series can do a lot to improve the signal integrity. The resistor should be sized so that the source resistance of the driver + the terminating resistor = characteristic impedance of the transmission line.
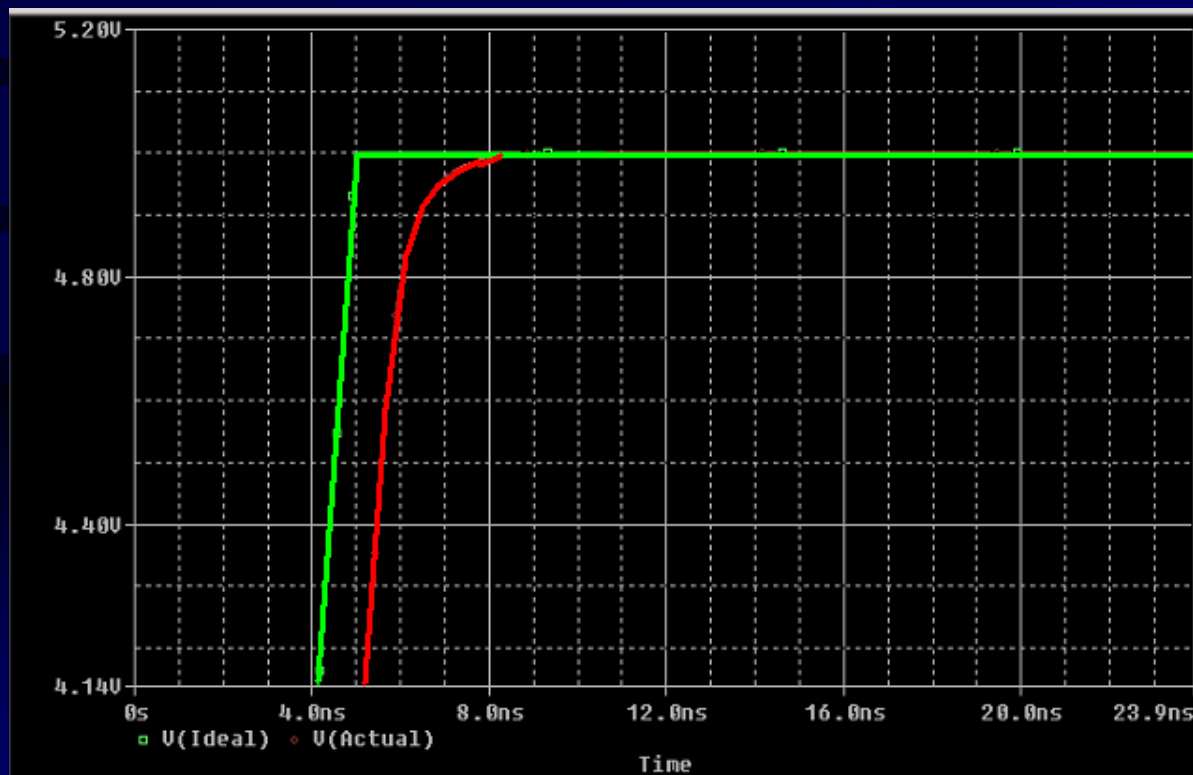
$$Rs + Rterm = Zo$$

- There are lots of transmission line impedance calculators on the web.

Transmission Line Source Termination Model
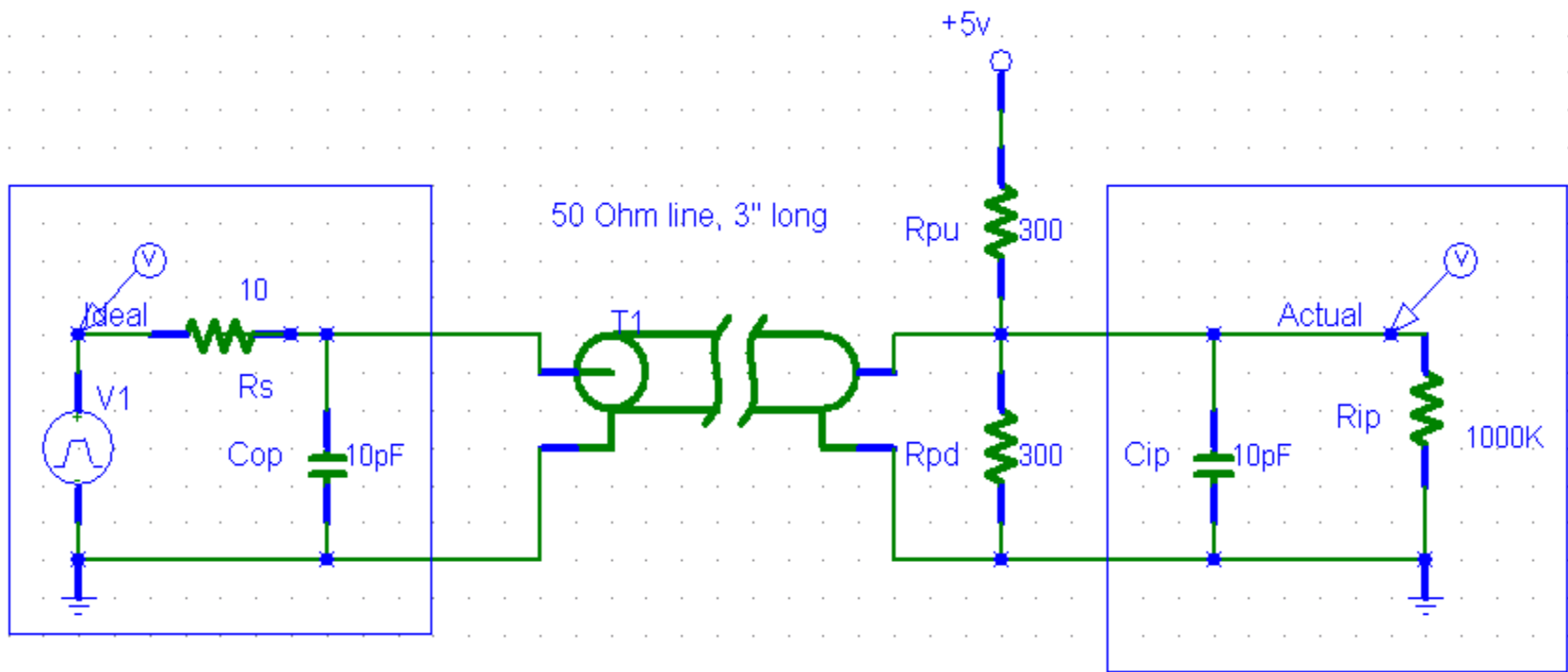
Transmission Line Source Termination

- The simulation shows that the overshoot and undershoot have been eliminated, due to the low pass filter.

Transmission Line Parallel Termination

- Source termination doesn't work for lines that drive multiple loads, so parallel termination at the last load is used.

- Ideally, Rpu || Rpd would equal the characteristic impedance of the transmission line, but most drivers can't source that much current.

Transmission Line Parallel Termination Model

# Transmission Line Parallel Termination

- The overshoot and undershoot have been attenuated, whether it's enough depends on your design.

Component placement

- Spend some time thinking about where to place major components, it will make routing much easier.
- Start with connectors, pushbuttons, etc. Their location is often fixed due to the function or form factor of the product.
- Pay attention to which components have lots of connections between them, try to orient the components so that the traces can be straightforward.
- Partition the board according to function, such as digital, analog and power supply. Try not to let traces from one section stray into another section.

Component Placement Example
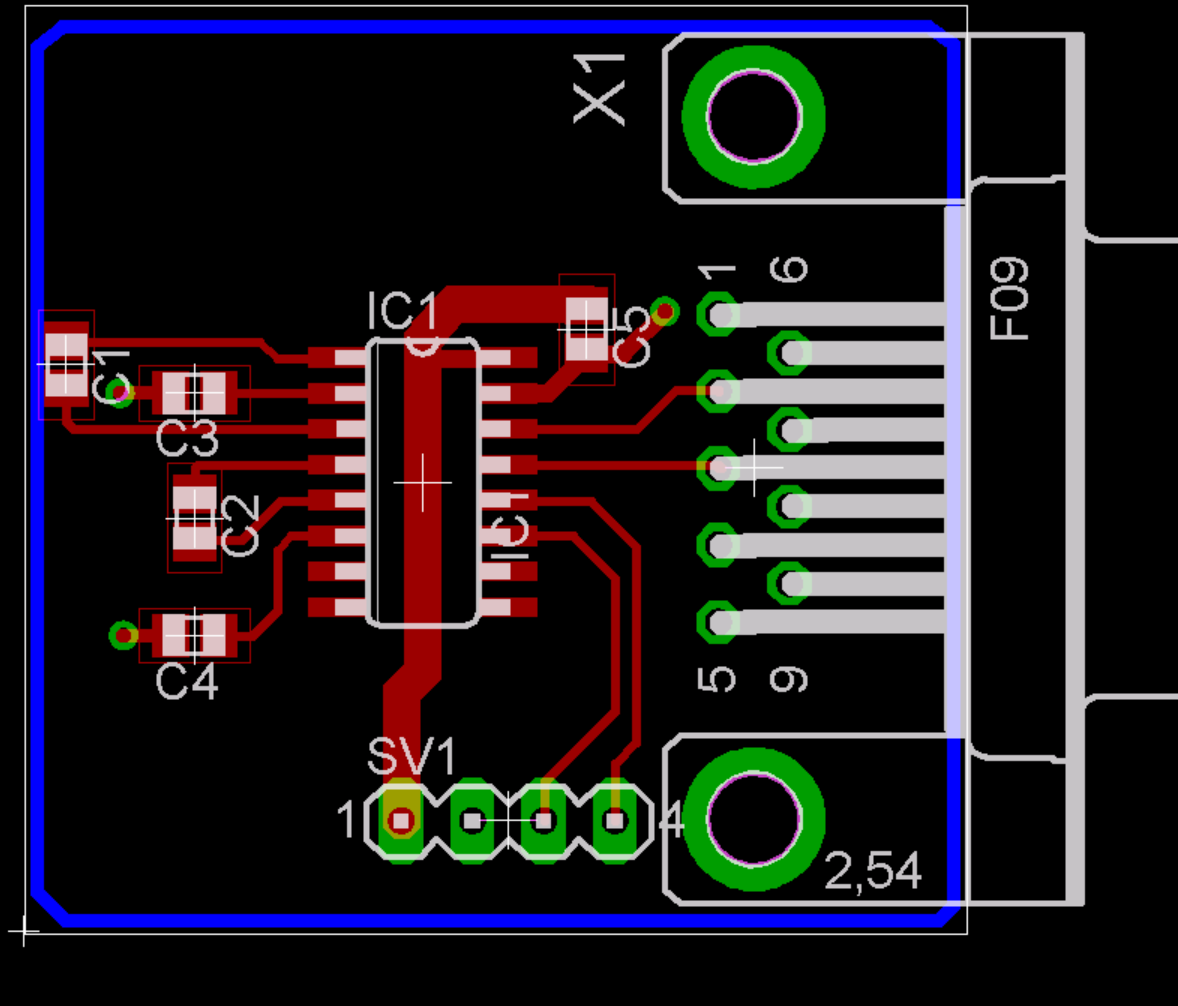
Critical Trace Routing

- Identify the most critical traces in the design: clock signals, analog signals, RF signals, etc. Route these traces first, with the most desirable layout.

- Maintain at least a 3X trace width separation around constantly switching traces like clocks (avoids crosstalk)

- You are smarter than the auto router software, so don't use it.

Safety considerations in routing

- Some traces have safety requirements.
  - AC & DC power inputs
  - Traces near connectors/openings in chassis
- Make high current traces large enough to safely handle the current required.
- Space out high voltage traces.
- Space out high voltage components with conductive housings.
  - Heat sinks
  - Electrolytic capacitors

PCB Specifications

- Minimum Line/Space Minimum   6 mils

- Maximum Hole Size   246 mils

- Minimum Hole Size   15 mils

- Only plated holes allowed

- Only top silkscreen allowed

- Manufacturing files in Gerber 274X format

- Maximum board size for demo price: 60 sq. inches

DFD: Design-For-Debug

- As board space allows, add features to the PCB that will help in debugging the design.
  - Unconnected headers for fixing board problems
  - Convenient power/gnd connections for scope probes
  - Test points for important subsystems (SPI bus, ADC, etc.)
  - Descriptive silkscreen
  - Extra LEDs, 7 segment display, serial port connection, speaker, etc..
- These extras can be no-loaded when you go to production.

PCB Checklist

- Do I have header pins for debugging?
- Do I have convenient VCC/GND test points?
- Do I have unconnected header pins for fixing board problems?
- Do I have mounting holes (both in schematic and board)?
- Have I printed out a paper version of the top copper and ensured that my parts fit the footprints?
- Do I have in-circuit programming for my CPU if it is surface mount?
- Do I have test plan for my board for when it comes back?